RESUME

Name: Dr. Mrs. Shaila Subbaraman.

Designation: Professor in Electronics Engineering (PG Side)

Date of Birth: 1 / 4 / 1950

Address: **Present:** 37, Saikrishna,
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Email:- :- s.subbaraman@gmail.com

Academic Qualification: (Starting from Graduation)

Degree	Year of Passing	University/ Institute	Subjects	Grade
B.Sc.	1970	Shivaji University	Physics	Distinction
M.Sc.	1973	Shivaji University	Physics (Materials Science)	I-class
M.Tech.	1975	I.I.Sc. Bangalore	Physical Engg. (Sp. :Solid State Electronics)	Distinction
Ph.D.	March, 1999	I.I.T. Bombay	Microelectronics	-
Diploma in Advanced VLSI Design	2001	C-DAC, Pune.	VLSI Design	B

Ph. D. Topic: "Radiation and hot carrier effects in submicron MOS devices" under the guidance of Prof. Dinesh Sharma at Indian Institute of Technology, Dept of Electrical Engineering, Mumbai

Teaching Experience:

Duration From	Duration To	College / University	Post Held	Main Subjects Taught
Aug.89	Dec.91	Walchand College of Engg.,Sangli (WCE, Sangli), Maharashtra, India	Lecturer	Digital Electronics, Electron Devices ,L.I.C.
Jan. 92	Jun 02		Assistant Professor	Micro-electronics, Microprocessor, Computer N/W, VLSI Design.
July 02	Dec 02		Professor	Computer N/W, VLSI Design.
Jan 03	June 05		H.O.D. (Electronics)	Computer N/W, VLSI Design.
July 05	Dec. 2010		Professor (P.G), Dean Academics	VLSI Design (P. G., U. G.), Electronic Circuit Design, Digital System Engineering
Jan 2011	May2011	WCE, Sangli, India DKIT, Ichalkaranji	Visiting Professor	CMOS VLSI Design, Computer Arch. DSP-VLSI, Digital System Engineering
Oct 2011	May 2012	WCE, Sangli, India	Professor (Contractual)	CMOS VLSI Design, DSP-VLSI
July 2012- Feb. 2014 March 2014 onwards		ADCET, Ashta, India WCE, Sangli	Professor Professor (Contractual)	CMOS VLSI, Design, Digital System Engineering DSP-VLSI, CMOS VLSI Design, Analog VLSI Design, Testing and Testability

Industrial Experience: (Training / Job)

Organization	Duration From	To	Post Held	Experience on
L.R.D.E. Bangalore	May 74	July 74	Trainee Engineer	PCB manufacturing,
Semiconductors Ltd Pune.	Aug. 75	March 83	Engineer.	Small signal semiconductor device manufacturing
I.T.M.C. R&D Center, Pune	April 83	Nov. 84	Sr. Engineer	High power rectifiers (R & D)
New Market Micro systems, Ltd U.K.	May 85	July 85	Trainee Engineer	TFHIC manufacturing and Quality Control
Western India Enterprises, Electronics Div. Pune	Dec. 84	Aug.89	Deputy Manager (Quality Control)	TFHIC manufacturing for telecomm and space electronics

- **Seminar/ Conferences/Short-term Courses Attended: 50 +**

- **Worked as resource person for various workshops/ short term courses/ guest lectures : 30+**
- **Expert lectures on NBA and OBE guidelines:** At various colleges in Maharashtra (CoE, Pune, SIT, Yedrav, DKTE, Ichalkaranji, Technology Department, SUK, Vidyalankar, Mumabi, SPIT, Mumbai, MIT, Aurangabad, TKIT, Warananagar, CoE, Karad),
- **Deputed by NPIU for delivering guidelines on NBA and OBE:** RGTU Bhopal, Jabalpur CoE, Jabalpur M.P., GCoE, Kalahandi, Odisha, PMEC, Beharampur, Odisha,, Kangra CoE, Himachal Pradesh etc.)
- **Working as institute NBA/NAAC coordinator** at Walchand College of Engineering, Sangli for UG amd PG courses.

Guidance to Ph. D. students : Ph D degree awarded: 6/10, Thesis Submitted : 1/4

o	Student	Year of Reg	Title	Status
1	Mr. B. G. Patil	2005	Human Feature Vector and Classifier Through IRIS Pattern Recognition	Degree awarded in July 2015
2	Mr. Prasad Khandekar	2007	Low power digital design using energy recovery adiabatic logic	Degree Awarded in Jan 2013
3	Mrs Sheetal Bhandari	2008	Performance Enhancement Using Reconfigurable Devices For Real-Time, Computationally Intensive Application	Degree awarded March 2013
4	Mrs. Anagha Khedkar	2007	Genetic Algorithm with Ramp Variation in Mutation to Discover the Goal Polynomial	Degree awarded in Jan 2015
5	Mrs. V. Jayashree	2007	Weaved Fabric Defect Detection Using Image Processing Techniques.	Degree awarded in March 2014
6	Mr. R.N. Patil	2007	Power Efficient Architecture for High Throughput Digital Systems.	Degree awarded in Dec 2017
7	Mrs. Jayshree Rudagi	2007	Low power CORDIC Processor	Thesis submitted
8	Mrs. Anjali Patil	2011	Guesture Analysis and synthesis	In Progress
9	Mrs. Deepali Loni	2012	Music Signal Analysis	In Progress
10	Mr. Rajan Devi	2012	Efficient Grid Distribution for Electrical Power	In Progress

Patent : Patent filed on 17th August 2011
Application No. 2315/MUM2011 dated 17/08/2011.
Title: "Pass Transistor Adiabatic Logic Circuit with Stand- By Mode (PAL2NSM)"

No. of M.E. students supervised so far : 34 Nos.

Dissertation Topics: in VLSI Design, VLSI-DSP, Image Processing

Details of Publications); The updated list with citationscan be obtained from Google Scholar.

International Journal Papers

1. S. Subbaraman, Dinesh Sharma, J. Vasi, "A Monte Carlo method to resolve the memory effect in switched gate bias experiments", Journal of Applied Physics, 83(6), 3419(1998)

2. Prasad Khandekar, Shaila Subbaraman, "Low power digital design using adiabatic recovery logic", International Journal of Engineering Research and Industrial Applications, Vol 1, No. III (2008), pp 199-208

3. Prasad Khandekar, Shaila Subbaraman **, "**Ultra-Low Power Quasi-Adiabatic Inverter", International Journal of Computational Intelligence Research and Applications, Vol. 3, No. 1 (2009), pp. 11-15

4. Jayashree Vaddin, Shaila Subbaraman, "Identification of plain grey fabric defects using DC suppressed Fourier power spectrum sum features", Accepted for publication in Melliand International Technische Textilien / Technical Textiles Melliand China CFI-China journal

5. Prasad Khandekar, Shaila Subbaraman **,** "Low Power Inverter and Barrel Shifter Design Using Adiabatic Principle (code no. Print: ISSN 0973-6107)", Advances in Computational Sciences and Technology (ACST). Research India Publications (Online ISSN 0974-4738)

6. Jayashree Vaddin, Shaila Subbaraman, "Identification of twill grey fabric defects using DC suppressed Fourier power spectrum sum features", Textile Research Journal, Vol 82, Number 14, Sept. 2012, Pg 1485-97, ISSN 0040-5175.

7. Anagha Khedkar, Shaila Subbaraman, " Effect of advanced twin operator on the performance of genetic algorithm", International journal of advanced research and technology. ISSN 0974-3154 Vil 3, No. 3 (2010), PP 721-731 (http:/www.irphouse.com)

8. Anagha Khedkar, Shaila Subbaraman, " Novel approach of varying mutation probability in genetic algorithm", International journal of systemic, cybernetics and informatics, April 2009, pg. 065

9. Prasad Khandekar, Shaila Subbaraman, " Optimal Conditions for Ultra Low Power Digital Circuits", Journal of Active and Passive Electronic Devices, 2011, Vol 6, pp 157-167 paper identifier no.RC081

10. Mr. Babasaheb G. Patil, Mr. Nikhil Niwas Mane, Dr. Mrs. Shaila Subbaraman, " Iris Feature Extraction and Classification using FPGA", Accepted for publication in Dec. 2011 issue

11. Sheetal Bhandari, Shaila Subbaraman, Shashank Pujari, " A Novel Reconfigurable Controller for speed Efficient Dynamic Partial Reconfiguration", International Journal on Advances in Computational Sciences and Technology, ISSN 093-6107,Vol 4(2),2011, PP 229-242.

12. S. Bhandari, S. Subbaraman, F. Cancare, F. Bruschi, M. D. Santambrogio, "An Efficienr Reconfiguration Manager for Dynamic Partial Reconfigurable FPGA based Architectures", under review at International Journal in Reconfigurable Computing, Hindwai Publications.

13. J. M. Rudagi, Srikant Basavraj, S. Subbaraman, " Performance Analysis of Radix 4 CORDIC Processor in Rotation mode with Parallel Scale Factor Computation" , International Journal of Emerging Technology and Advanced engineering- ijetae (ISSN 2250-2459, Vol.2, Issue 7

14. V. Jayshree, S. Subbaraman, "DCSFPSS based Tribrid Approach for In-Process Quality Check in Textiles", to be submitted to IEEE transactions or Textile research Journal

15. Mrs. A. R. Patil, S. Subbaraman, "A Review on Vision Based Hand Gesture Recognition Approach Using Support Vector Machines", IOSR Journal of Electronics and Communication Engineering, ISSN:2278-2834, ISBN:2278-8735, PP 07-12, Dec 2012

16. Anagha Khedkar, Shaila Subbaraman , "The Novel Approach of Adaptive Twin Probability for Genetic Algorithm", International Journal of advanced studies in Computer, Science and Engineering (IJASCSE), Volume 2, Special Issue 2, September 2013

National Journal Papers

1. Sheetal Bhandari, Shaila Subbaraman, Shashank Pujari, " Internal dynamic partial reconfiguration for real time signal processing on FPGA" , Indian Journal of Science and Technology , Vol. 3 , No.4, April 2010, pg 365-368

2. Prasad Khandekar, S.Subbaraman, "Low Power Inverter and Barrel Shifter Design Using Adiabatic Principle" , (code no. Print: ISSN 0973-6107 Online ISSN 0974-4738), Advances in Computational Sciences and Technology (ACST) , Research India Publications 2008

Besides these journal papers there are publications through presentations in various national and international conferences, a summary of which is as given below. (Refer Google Scholar Citation attached herewith.)

Summary :

Journal		**Conference**	
International	National	International	National
16	2	35	33

Other Information:-

1. **P.G. and Ph. D. guide** recognition of Shivaji University, Kolhapur, India for the discipline of Electronics Engineering.

2. **Worked as NBA (National Board of Accreditation) expert committee member during 2012-18 for inspecting colleges in various states of India viz. Uttar Pradesh, Andra Pradesh and Tamilnadu in accordance with Outcome Based Education philosophy in line with ABET criteria.**

3. **Worked as AICTE expert committee member during 2012-18 for inspecting engineering and management colleges in various states of India viz. Uttar Pradesh, Madhya Pradesh, Himachal Pradesh, Punjab .**

4. **Have been assigned the duty from Feb 2018 of educating the faculty of various engineering colleges/ universities from Himachal Pradesh, Madhya Pradesh, Odisha etc by NPIU (A Govt of India organization), New Delhi, India to equip them with OBE practices.**

5. **Have provided OBE and accreditation related guidance to number of engineering colleges in Maharashtra. These colleges have successfully implemented OBE practices and many of their programs have been accredited by NBA, India.**

6. **Have presented 2 papers in national conferences and one paper in international conference based on outcome based education philosophy.**

7. **Was felicitated by Trans-Asia Chamber of Commerce and Industry for Pillars of Hindustani award in Feb 2017 for contribution in Higher Education. .**

8. Was nominated as coordinator for **Asia-Link project** on behalf of India which had members participating from six countries viz. Italy, Germany, India, Sri Lanka, Thailand and Vietnam. One of Ph. D. students interacted with the Chief Investigator of this project viz Dr. Marco Santambrogio from Politechnico Di Milano, Italy and worked there for three months to complete her Ph D.

9. Was nominated for **Technomentor Award- 2008** instituted by Indian Semiconducor Association and VLSI Society of India in 2008.

10. Have received " Gungaurav Ideal Professor Award" instituted by Shikshan Mandal, Karad, Maharashtra in 2016 for the efficient services rendered in higher education for more than 25 years.

11. Worked as a **Member of Board of Studies** for Bharati Vidyapeeth, Board of Electronics and Telecommunication, Pune, Ramatirth Marathwada University, Board of Instrumentation, Nanded, International institute of Information Technology, Board of VLSI and Microelectronics , Pune during 2008-10

12. Worked as RR committee member of Pune University for Electronics Engineering,(2013-15) and of Shivaji University, Kolhapur from 2008-11

13. Worked as a **department Head** for Dept. of Electronics Engineering, WCE, Sangli, Maharashtra from Jan. 2003 to June 2005.

14. Worked as the first Dean Academics of autonomous Walchand College of Engg., Sangli, Maharashtra, from July 2005 till March 2010. I played an importance role in setting the various academic practices in the college successfully.

15. Prepared and presented proposal to **DST, Govt. of India, under FIST** (**F**unds for **I**nfrastructure development of **S**cience and **T**echnology) scheme and sought a grant **of Rs. 25 lakhs** for the Electronics Engineering department of WCE, Sangli, Maharashtra.

16. Handled the **AICTE funded research project** on Development of Digital Neuron Chip (Funds **of Rs. 10 lakhs**)- 2003-2006

17. Have worked as a **review committee member** for reviewing the technical papers for VDAT-O5 (National level conference on VLSI Design and Embedded system design) and also for McGraw **Hill's** books on Electronic Devices and Circuits by Millman and Halkias and VLSI books by Indian authors. Also have reviewed a couple of papers for the conferences held abroad.

18. Worked as a visiting faculty for International Institute of Information Technology, Pune (2005-07) for delivering a series of guest lectures on low power CMOS design. And Mody University, Rajasthan for entire course on CMOS VLSI Design in 2014-15.

19. **Industry experience** in various capacities (Engineer, Senior Engineer, Deputy Manager) for 14 years in semiconductor device/IC manufacturing industries in Pune before joining Walchand College of Engineering, Sangli.

    a. Worked in
        i. Production department of Small signal devices (Semiconductors Ltd., Pune) for 8 years (1975-83),
        ii. R & D department of ITMC R & D Center , Pune (AOL group) on High Power Rectifiers(400 A/3000V)for 1and 1/2 years (April 1983- Nov 1984),
        iii. Quality Control department of Electronics Division of Western India Enterprises (WIE), Ltd., Pune on Thick Film Hybrid Integrated Circuits for four and half years (Dec 1984 – Aug. 1989)
    b. While in WIE, Pune,
        i. I interacted closely with Q/C group of Indian Space Research Organization, Bangalore for manufacturing quality hybrid circuits for their space program.
        ii. Also I got an opportunity to work and receive training on Quality Control aspects of manufacturing of Thick film hybrid microcircuits in Newmarket Microsystems Ltd., UK for 2 months in 1985.
        iii. The job profile experience in industries helped me to acquire the observational, analytical, communication and documentation skills which are helping me even today in academics to impart those effectively to other faculty members of parent as well as other institutes as well as the students.

Strengths and Weaknesses:

Strengths:	**Weaknesses:**
1. Industrial and academic exposure	1. Workaholic
2. Dedication and hard work	2. Taking anything too seriously
3. Research inclination	3. Expecting perfection in all

Dr. Mrs. Shaila Subbaraman